APDS-9200

Digital UV and Ambient Light Sensor

Data Sheet

Description

The Broadcom APDS-9200 device provides ultra-violet (UV-A and UV-B) sensing and ambient light sensing in a specially designed matrix arrangement for optimization. This allows the device to have optimal angular response for ultra-violet and ambient light sensing. The APDS-9200 converts UV light into digital data and display as UV index (1… >11) with higher values representing higher UV exposures.

The ultra-violet sensing feature is useful in consumer applications for monitoring of UV-A and UV-B radiation as UV radiation is part of the electromagnetic spectrum that reaches the earth from the sun. APDS-9200 is able to measure UV wavelength which has been classified into UV-A (320 nm – 400 nm) and UV-B (290 nm – 320 nm). The ambient light sensing is targeted for display management with the purpose of extending battery life and offers optimum viewing in diverse lightning conditions.

APDS-9200 supports the I^2C interface and has a programmable interrupt function that frees up micro-controller resources using upper and lower thresholds events.

Ordering Information

Part Number	Packaging	Quantity
APDS-9200	Tape and Reel	2500 per reel

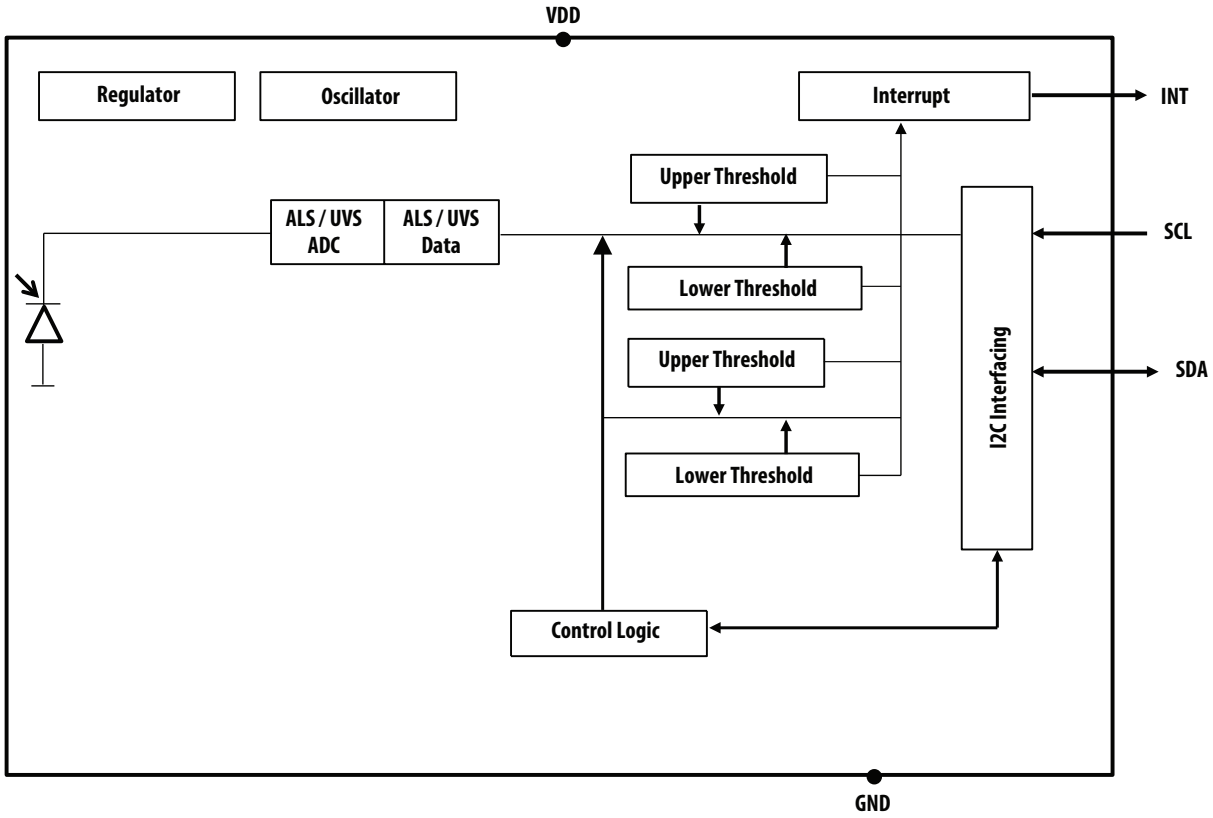
Features

- Ultra-Violet (UV-A and UV-B) and ambient light sensing
  - Digital UV Index register (1 … > 11)
  - Linear output
  - Excellent temperature compensation
- Ambient Light Sensing (ALS)
  - Utilizes coating technology to emulate human eye spectral response (V-Lamda characteristics)
  - High sensitivity in low lux condition – Ideally suited for operation behind dark glass
  - Low lux performance at 0.008 lux
  - Up to 20-bit resolution
- I^2C Interface Compatible
  - Up to 400 kHz (I^2C Fast-Mode)
  - Dedicated interrupt pin
- Small package: L 2.0 mm × W 2.0 mm × H 0.65 mm

Applications

- Ultra-violet and Ambient Light Sensing
- Mobile devices – cell phones, tablets, outdoor navigation display
- Wearable devices – smart watch, sport watch

Figure 1 Functional Block Diagram



Detailed Description

The APDS-9200 device contains multiple photodiodes for UV and Ambient Light Sensing as well as temperature compensation that are designed in a matrix placement to achieve optimum angular response at the fall of incident light angle. The photodiode currents are converted to digital count by ADCs. The ADC resolution is selected from 13 bits to 20 bits and the conversion time is inversely proportional to the ADC resolution. The device is connected by an I^2C interface to a microcontroller through a set of registers. APDS-9200 has a programmable interrupt with hysteresis to respond to events which will reduce the microcontroller tasks with upper and lower thresholds. The device includes a circuit for an internal oscillator, a current source, voltage reference, and internal nonvolatile memory (NVM) to store trimming information.

The UV light sensor has to be operated independently from Ambient Light Sensor. To enable the reading of UV sensor, UVS_MODE and LS_EN bit has to be correctly set in the MAIN_CTRL register. Setting the UVS_MODE bit will stop a running ALS measurement and start a new UV sensor reading.

Table 1 I/O Pins Configuration

Pin	Name	Type	Description
1	SCL	I	I^2C serial clock input terminal — clock signal for I2C serial data
2	SDA	I/O	I^2C serial data I/O terminal – serial data I/O for I2C
3	VDD	Supply	Power Supply Voltage
4	INT	O	Interrupt – Open drain
5	NC		No Connect
6	GND	Ground	Power supply ground. All voltages are referenced to GND

Table 2 Absolute Maximum Ratings over Operating Free-Air Temperature Range (unless Otherwise Noted)

Parameter	Symbol	Min.		Max.	Units	Conditions
Power supply voltage	V_{DD}			4.0	V	All voltages are with respect to GND.
Max voltage on SCL, SDA, INT pads	V_{I2C}	0.5		4.0	V	
Storage temperature	T_{stg}	–40		95	°C	

Table 3 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating ambient temperature	T_A	–40		85	°C
Supply voltage	V_{DD}	1.7		3.6	V
Supply Voltage accuracy, VDD total error including transients		–3		3	%

Table 4 Electrical Parameters, T_A=25°C (unless Otherwise Noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
ALS Active mode current	I_{ALS}	V_{DD} = 2.8V, Gain Mode 3		110		µA
UV Active mode current	I_{UV}	V_{DD} = 2.8V		100		µA
Standby current	I_{STBY}	In Standby Mode. No active I^2C communication		1	2	µA
SCL, SDA input high voltage	V_{IH}		1.5		V_{DD}	V
SCL, SDA input low voltage	V_{IL}		0		0.4	V
VOL INT, SDA output low voltage			0		0.4	V
ILEAK leakage current, SDA, SCL, INT pins	ILEAK		–5		5	µA

Table 5 ALS/UV Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Dark count		Lux=0, 18 bit range		0		counts
Min integration time	$T_{intmin1}$			3.125		ms
	Ti_{ntmin2}	With 50/60Hz rejection		50		ms
Max integration time	T_{intmax}	With 50/60Hz rejection		400		ms
ALS output resolution	RES_{ALS}	Programmable	13	18	20	bits
UV output resolution	RES_{UV}	Programmable	13	18	20	bits
ADC count value		Intensity = 121 µW/cm^2 with 310 nm light source, GAIN = 18×, resolution = 20 bits, V_{DD} = 2.8V		1700		counts
ALS/UV repeat rate		Programmable	25		2000	ms

Figure 2 ALS Spectral Response

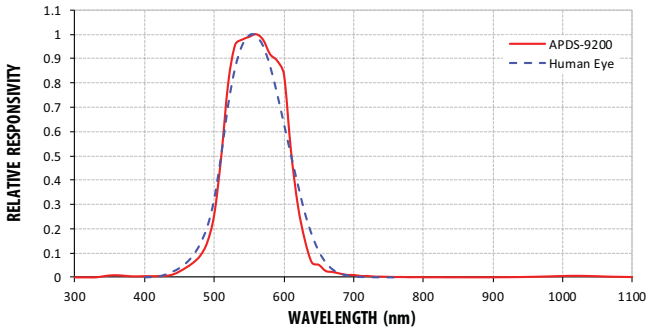


Figure 3 UV Spectral Response

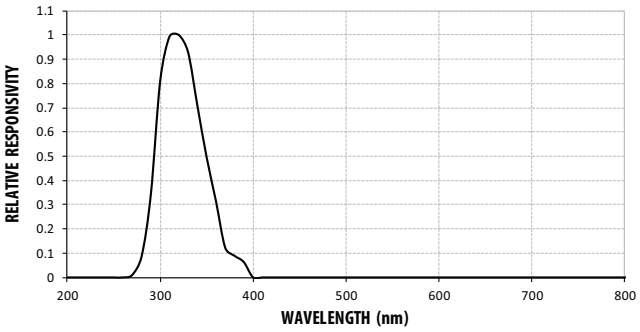


Figure 4 ALS Sensor LUX vs. Meter LUX using White Light

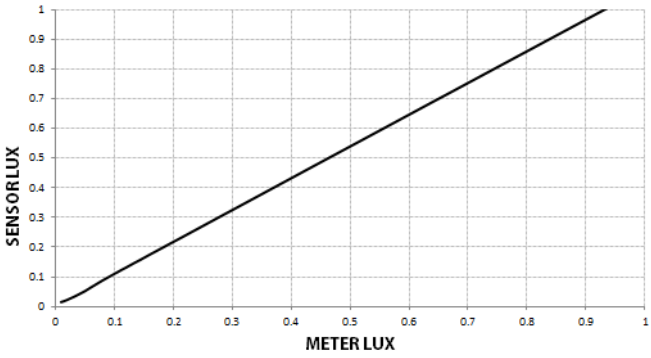


Figure 5 ALS Sensor LUX vs. Meter LUX using White Light

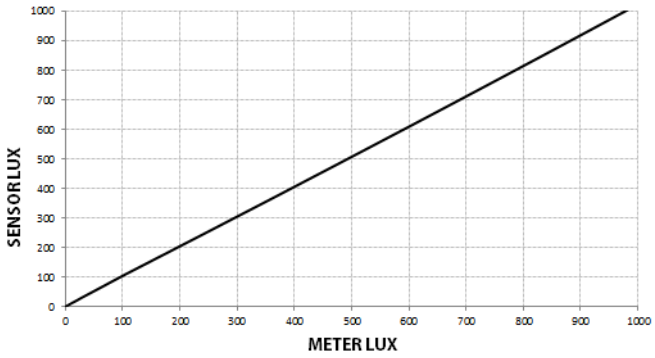


Figure 6 ALS Sensor LUX vs. Meter LUX using Incandescent Light

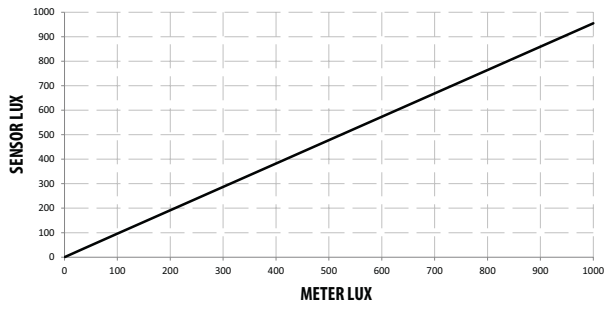


Figure 7 UV Sensor Count vs. UV Meter Index (310 nm UV Source)

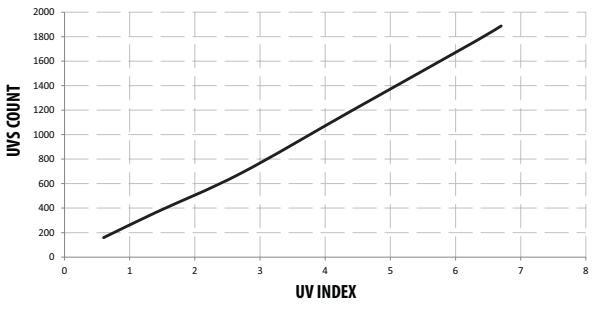


Figure 8 Normalized Standby IDD vs. VDD

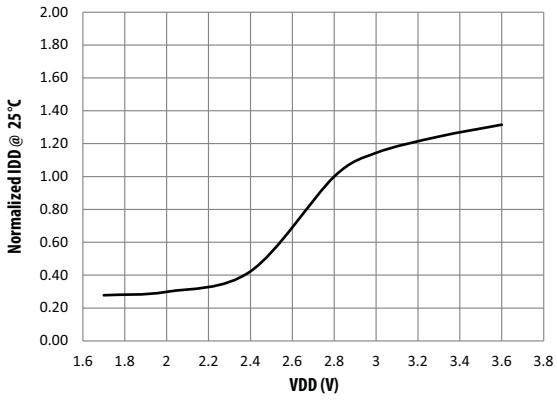


Figure 9 Normalized Standby IDD vs. Temperature

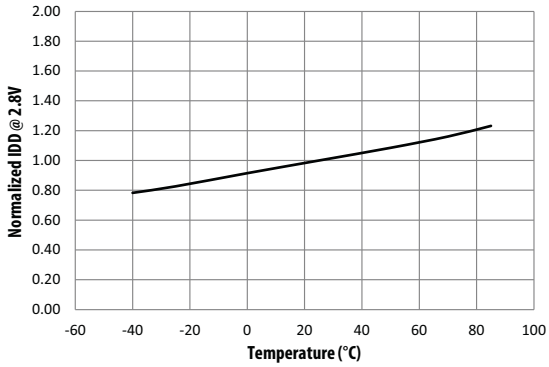


Figure 10 Normalized ALS Data Count @ 1000Lux White LED vs. VDD

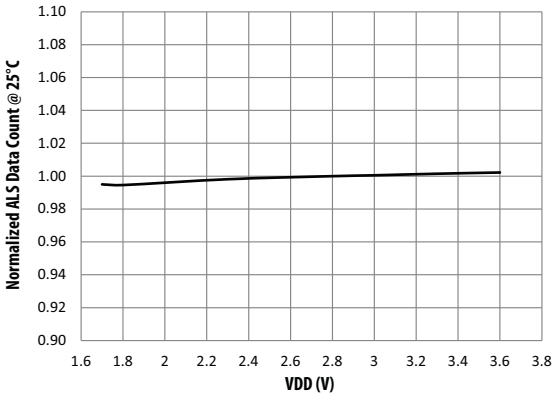


Figure 11 Normalized UVS Data Count @ 121 µW/cm^2 (310 nm) vs. VDD

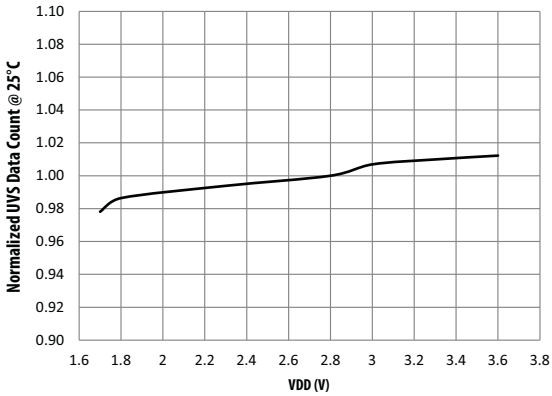


Figure 12 Normalized ALS Data Count @ 2.8V vs. Temperature

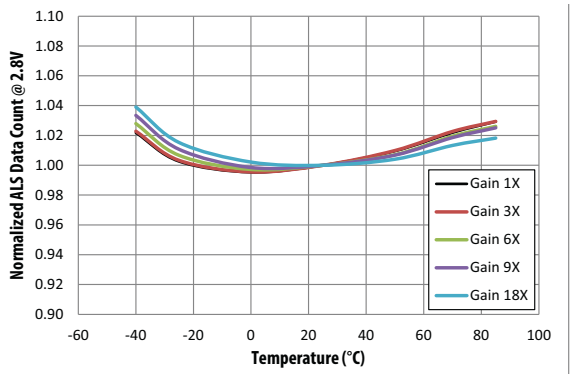


Figure 13 Normalized UVS Data Count @ 121 µW/cm^2 (310nm) VDD = 2.8V vs. Temperature

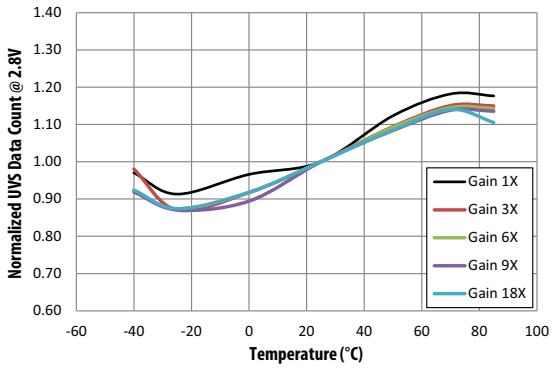


Figure 14 Normalized ALS Responsitivity vs. Angular Displacement

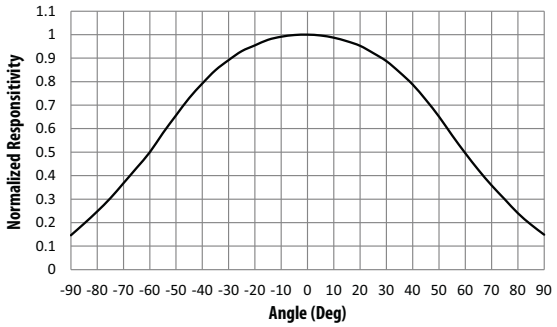
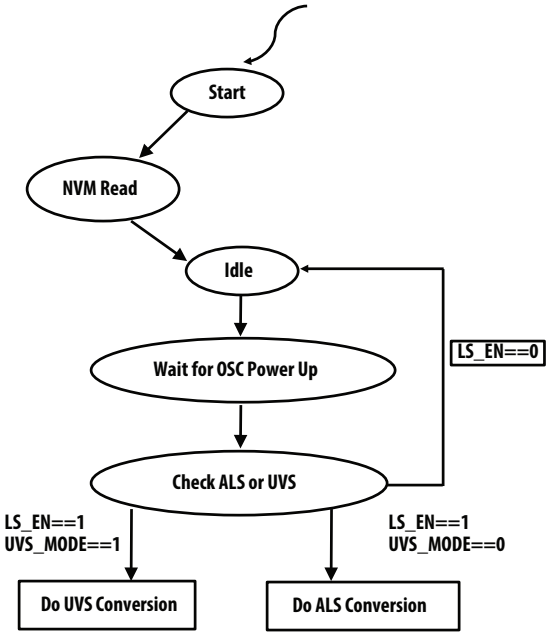


Figure 15 System State Machine



Start Up after Power-On or Software Reset

The main state machine is set to "Start State" during power-on or software reset. As soon as the reset is released, the internal oscillator is started and the programmed I^2C address and the trim values are read from the internal trimming data block. The APDS-9200 enters Standby Mode as soon as the idle state is reached.

NOTE As long as the I^2C address has not yet been read, the device will respond with NACK to any I^2C command and ignore any request to avoid responding to a wrong I^2C address.

Standby Mode

Standby Mode is the default mode after power-up. In this state, the oscillator, all internal support blocks, and the ADCs are switched off but I^2C™ communication is fully supported.

ALS and UVS Operation

ALS measurements can be activated by setting the LS_EN bit to 1 and the UVS_Mode bit to 0 in the MAIN_CTRL register.

UV measurements can be activated by setting the LS_EN bit to 1 and the UVS_Mode bit to 1 in the MAIN_CTRL register.

As soon as ALS or UVS become activated through an I^2C command, the internal support blocks are powered on. Once the voltages and currents are settled (typically after 5 ms), the state machine checks for trigger events from a measurement scheduler to start the ALS or UVS conversions according to the selected measurement repeat rates.

Once LS_EN is changed back to 0, a conversion running on the respective channel will be completed and the relevant ADCs and support blocks will move to standby mode.

Interrupt Features

APDS-9200 generates independent Light sensor (ALS/UVS depend on configuration) interrupt signal that can be multiplexed and output to the INT pad. The interrupt conditions are always evaluated after completion of a new conversion on the LS channels.

Light Sensor Interrupt

The LS interrupt is enabled by LS_INT_EN = 1. It can function as either threshold triggered (LS_VAR_MODE = 0) or variance trigged (LS_VAR_MODE = 1). The LS interrupt source generator either uses the ALS_DATA or the UVS_DATA registers at input. The LS interrupt source is selected by the LS_INT_SEL bits in the INT_CFG register.

The Light Sensor threshold interrupt is enabled with LS_INT_EN = 1 and LS_VAR_MODE = 0. It is set when the data of the selected LS_DATA input register (ALS_DATA or UVS_DATA) is above the upper or below the lower threshold for a specified number of consecutive measurements.

The Light Sensor variance interrupt is enabled with LS_INT_EN = 1 and LS_VAR_MODE = 1. It is set when the absolute value of the difference between the previous and current LS_DATA data value is above the decoded LS variance threshold for a specified number of consecutive measurements.

I²C Protocol

Interface and control of the APDS-9200 is accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The device supports a single slave address of 0x52 hex using 7 bit addressing protocol. (Contact the factory for other addressing options.)

I²C Register Read

The registers can be read individually or in block read mode. When two or more bytes are read in block read mode, reserved register addresses are skipped and the next valid address is referenced. If the last valid address has been reached, but the master continues with the block read, the address counter in the device will not roll over and the device returns 00HEX for every subsequent byte read.

The block read operation is the only way to ensure correct data read out of multi-byte registers and to avoid splitting of results with HIGH and LOW bytes originating from different conversions. During block read access on LS result registers, the result update is blocked.

If a read access is started on an address belonging to a non-readable register, the APDS-9200 will re-turn NACK until the I²C operation is ended.

Read operations must follow the timing diagram in Figure 16.

I²C Register Write

The APDS-9200 registers can be written to individually or in block write mode. When two or more bytes are written in block write mode, reserved registers and read-only registers are skipped. The transmitted data is automatically applied to the next writable register. If a register includes read (R) and read/write (RW) bits, the register is not skipped. Data written to read-only bits are ignored.

If the last valid address of the APDS-9200 address range is reached but the master attempts to continue the block write operation, the address counter of the APDS-9200 will not roll over. The device will return NACK for every following byte sent by the master until the I²C™ operation is ended.

If a write access is started on an address belonging to a non-writeable register, the APDS-9200 will return NACK until the I²C™ operation is ended.

Write operations must follow the timing diagram in Figure 17.

Figure 16 I²C Register Read

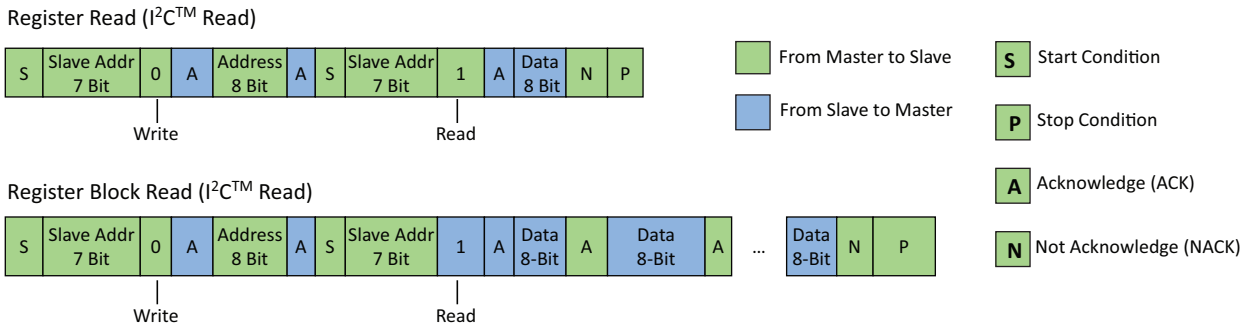


Figure 17 I²C Register Write

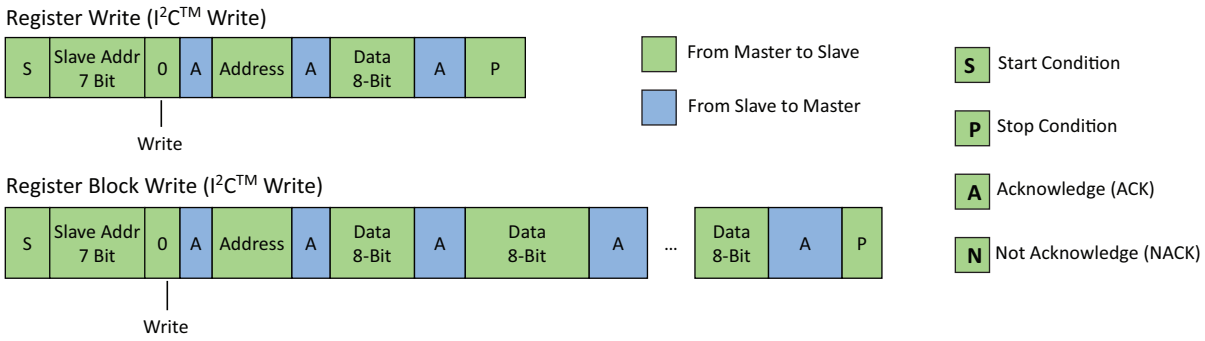


Figure 18 I²C Interface – Bus Timing

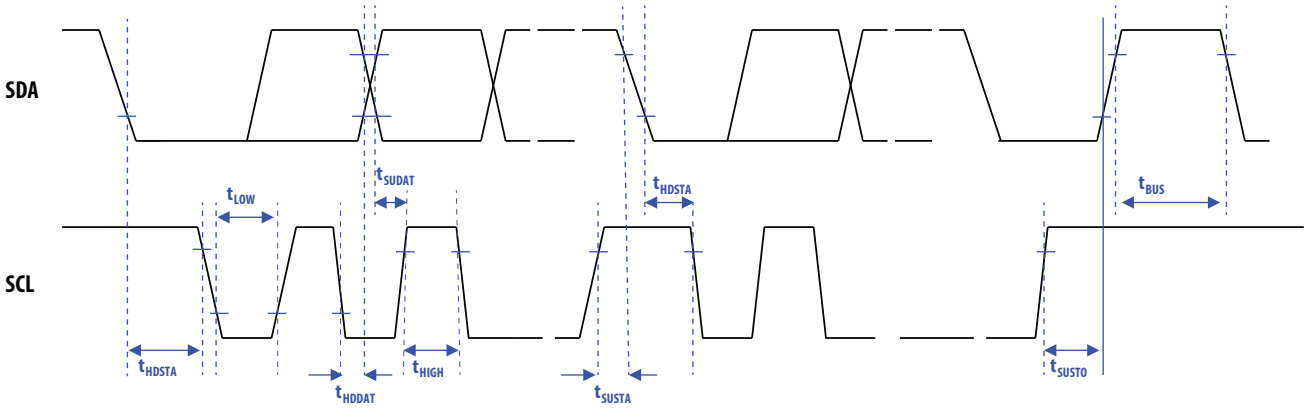


Table 6 Bus Timing Characteristics

Parameter	Symbol	Standard Mode	Fast Mode	Units
Maximum SCL Clock Frequency	f_{SCL}	100	400	KHz
Minimum START Condition Hold Time Relative to SCL Edge	t_{DSTA}	4		µs
Minimum SCL Clock Low Width	t_{LOW}	4.7		µs
Minimum SCL Clock High Width	t_{HIGH}	4		µs
Minimum START Condition Setup Time Relative to SCL Edge	t_{SUSTA}	4.7		µs
Minimum Data Hold Time on SDA Relative to SCL Edge	t_{HDDAT}	0		µs
Minimum Data Setup Time on SDA Relative to SCL Edge	t_{SUDAT}	0.1	0.1	µs
Minimum STOP Condition Setup Time on SCL	t_{SUSTO}	4		µs
Minimum Bus Free Time Between Stop Condition and Start Condition	t_{BUS}	4.7		µs

Register Set

The APDS-9200 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

NOTE Light Sensor (LS) refers to Ambient Light Sensor (ALS) or UV Sensor (UVS).

Table 7 Register Set

Address	Type	Name	Description	Reset Value
00HEX	RW	MAIN_CTRL	LS operation mode control, software (SW) reset	00HEX
04HEX	RW	LS_MEAS_RATE	LS measurement rate and resolution in active mode	22HEX
05HEX	RW	LS_GAIN	LS analog gain range	01HEX
06HEX	R	PART_ID	Part number ID and revision ID	B1HEX
07HEX	R	MAIN_STATUS	Power-on status, interrupt status, data status	20HEX
0DHEX	R	ALS_DATA_0	ALS ADC measurement data, LSB	00HEX
0EHEX	R	ALS_DATA_1	ALS ADC measurement data	00HEX
0FHEX	R	ALS_DATA_2	ALS ADC measurement data, MSB	00HEX
10HEX	R	UVS_DATA_0	UVS ADC measurement data, LSB	00HEX
11HEX	R	UVS_DATA_1	UVS ADC measurement data	00HEX
12HEX	R	UVS_DATA_2	UVS ADC measurement data, MSB	00HEX
13HEX	R	UVS_COMP_DATA_0	UVS COMP ADC measurement data, LSB	00HEX
14HEX	R	UVS_COMP_DATA_1	UVS COMP ADC measurement data	00HEX
15HEX	R	UVS_COMP_DATA_2	UVS COMP ADC measurement data, MSB	00HEX
16HEX	R	COMP_DATA_0	COMP ADC measurement data, LSB	00HEX
17HEX	R	COMP_DATA_1	COMP ADC measurement data	00HEX
18HEX	R	COMP_DATA_2	COMP ADC measurement data, MSB	00HEX
19HEX	RW	INT_CFG	Interrupt configuration	10HEX
1AHEX	RW	INT_PERSISTENCE	Interrupt persist setting	00HEX
21HEX	RW	LS_THRES_UP_0	LS interrupt upper threshold, LSB	FFHEX
22HEX	RW	LS_THRES_UP_1	LS interrupt upper threshold, intervening bits	FFHEX
23HEX	RW	LS_THRES_UP_2	LS interrupt upper threshold, MSB	0FHEX
24HEX	RW	LS_THRES_LOW_0	LS interrupt lower threshold, LSB	00HEX
25HEX	RW	LS_THRES_LOW_1	LS interrupt lower threshold, intervening bits	00HEX
26HEX	RW	LS_THRES_LOW_2	LS interrupt lower threshold, MSB	00HEX
27HEX	RW	LS_THRES_VAR	LS interrupt variance threshold	00HEX

MAIN_CTRL

Default Value: 00HEX

7	6	5	4	3	2	1	0	
0	0	0	SW-Reset	UVS_Mode	0	LS_EN	0	0X00

Field	Bit	Description
SW_Reset	4	1 = Reset will be triggered
UVS_Mode	3	0 = ALS 1 = UVS + compensation channels activated only
LS_EN	1	1 = ALS or UVS active 0 = ALS or UVS standby

LS_MEAS_RATE

Default Value: 22HEX

7	6	5	4	3	2	1	0	
0	LS Resolution/Bit Width			0	LS Measurement Rate			0X01

Field	Bit	Description
LS Resolution / Bit Width	6:4	000: 20 bit – 400 ms 001: 19 bit – 200 ms 010: 18 bit – 100 ms (default) 011: 17 bit – 50 ms 100: 16 bit – 25 ms 101: 13 bit – 3.125 ms 110: Reserved 111: Reserved
LS Measurement Rate	2:0	000: 25 ms 001: 50 ms 010: 100 ms (default) 011: 200 ms 100: 500 ms 101: 1000 ms 110: 2000 ms 111: 2000 ms

When the measurement repeat rate is programmed to be faster than possible for the specified ADC measurement time, the repeat rate will be lower than programmed (maximum speed).

Writing to this register stops the ongoing measurements and starts new measurements (depends on the respective bit).

ALS_GAIN and UVS_Gain

Default Value: 01HEX

7	6	5	4	3	2	1	0	
0	0	0	0	0	Gain Range			0X05

Field	Bit	Description
LS Gain Range (ALS Mode)	2:0	000: Gain 1 001: Gain 3 (default) 010: Gain 6 011: Gain 9 100: Gain 18
LS Gain Range (UVS Mode)	2.0	000: Gain 1 001: Gain 3 (default) 010: Gain 6 011: Gain 9 100: Gain 18

Writing to this register stops the ongoing measurements and starts new measurements (depends on the respective bit).

PART_ID

Default Value: B1HEX

7	6	5	4	3	2	1	0	
Part ID				Revision ID				0X06

Field	Bit	Description
Part Number ID	7:4	Part number ID
Revision ID	3:0	Revision ID of the component.

MAIN_STATUS

Default Value: 20HEX

7	6	5	4	3	2	1	0	
0	0	Power On Status	LS Interrupt Status	LS Data Status	0	0	0	0X07

Field	Bit	Description
Power On status	5	1 = Part went through a power-up event, either because the part was turned on or because there was power supply disturbance. All interrupt threshold settings in the registers have been reset to power-on default states and should be examined if necessary. The flag is cleared after the register is read.
LS Interrupt status	4	0: Interrupt condition not fulfilled (default) 1: Interrupt condition fulfilled (cleared after read)
LS Data status	3	0: old data, already read (default) 1: new data, not yet read (cleared after read)

ALS_DATA

Default Value: 00HEX, 00HEX, 00HEX

7	6	5	4	3	2	1	0	
ALS_Data_0 [7:0]								0X0D
ALS_Data_1 [15:8]								0x0E
0	0	0	0	ALS_Data_2 [19:16]				0X0F

ALS channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

The ALS channel output is already temperature compensated internally: ALS_DATA = (ALSint – COMP).

When an I^2C™ read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^2C™ read operation is completed or this address range is left.

This guarantees that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual ALS_DATA registers are updated as soon as there is no on-going I^2C™ read operation to the address range 07HEX to 18HEX.

Reg 0DHEX	Bit[7:0]	ALS diode data least significant data byte
Reg 0EHEX	Bit[7:0]	ALS diode data intervening data byte
Reg 0FHEX	Bit[3:0]	ALS diode data most significant data byte

UVS_DATA

Default Value: 00HEX, 00HEX, 00HEX

7	6	5	4	3	2	1	0	
UVS_Data_0 [7:0]								0X10
UVS_Data_1 [15:8]								0x11
0	0	0	0	UVS_Data_2 [19:16]				0X12

UVS channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

The UVS channel output is already temperature compensated internally: UVS_DATA = (UVint – UVS_COMP)

When an I^{2}C™ read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^{2}C™ read operation is completed or this address range is left.

This guarantees that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual UVS_DATA registers are updated as soon as there is no on-going I^{2}C™ read operation to the address range 07HEX to 18HEX.

Reg 10HEX	Bit[7:0]	UVS diode data least significant data byte
Reg 11HEX	Bit[7:0]	UVS diode data intervening data byte
Reg 12HEX	Bit[3:0]	UVS diode data most significant data byte

UVS_COMP_DATA

Default Value: 00HEX, 00HEX, 00HEX

7	6	5	4	3	2	1	0	
UVS_Comp_Data_0 [7:0]								0X13
UVS_Comp_Data_1 [15:8]								0x14
0	0	0	0	UVS_Comp Data_2 [19:16]				0X15

UVS Compensation Channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned). The UVS Comp Channel data is clipped at (2Resolution – 1).

When an I^{2}C™ read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^{2}C™ read operation is completed or this address range is left.

This guarantees that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual UVS_COMP_DATA registers are updated as soon as there is no on-going I^{2}C™ read operation to the address range 07HEX to 18HEX.

Reg 13HEX	Bit[7:0]	UVS Comp diode data least significant data byte
Reg 14HEX	Bit[7:0]	UVS Comp diode data intervening data byte
Reg 15HEX	Bit[3:0]	UVS Comp diode data most significant data byte

COMP_DATA

Default Value: 00HEX, 00HEX, 00HEX

7	6	5	4	3	2	1	0	
Comp_Data_0 [7:0]								0X16
Comp_Data_1 [15:8]								0x17
0	0	0	0	Comp_Data_2 [19:16]				0X18

ALS compensation channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned). The compensation channel data is clipped at (2Resolution – 1).

If an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^2C read operation is completed or this address range is left.

This guarantees that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual COMP_DATA registers are updated as soon as there is no on-going I^2C read operation to the address range 07HEX to 18HEX.

Reg 16HEX	Bit[7:0]	ALS Comp diode data least significant data byte
Reg 17HEX	Bit[7:0]	ALS Comp diode data intervening data byte
Reg 18HEX	Bit[3:0]	ALS Comp diode data most significant data byte

INT_CFG

Default Value: 10HEX

7	6	5	4	3	2	1	0	
0	0	LS Interrupt Source		LS Variation Interrupt Mode	LS Interrupt Enable	0	0	0X19
0	0	LS_INT_SEL		LS_VAR_ MODE	LS_INT_EN	0	0	

FIELD	BIT	DESCRIPTION
LS_INT_SEL	5:4	00: IR Channel 01: ALS Channel (default) 10: Reserved 11: UVS Channel
LS_VAR_MODE	3	0: LS Threshold Interrupt Mode (default) 1: LS Variation Interrupt Mode
LS_INT_EN	2	0: LS Interrupt Disabled (default) 1: LS Interrupt Enabled

INT_PERSISTENCE

Default Value: 00HEX

7	6	5	4	3	2	1	0	
LS_PERSIST				0	0	0	0	0X1A

FIELD	BIT	DESCRIPTION
LS_PERSIST	7:4	0000: Every LS value out of threshold range (default) asserts an interrupt. 0001: 2 consecutive LS values out of threshold range assert an interrupt. … 1111: 16 consecutive LS values out of threshold range assert an interrupt.

LS_THRES_UP

Default Value: FFHEX, FFHEX, 0FHEX

7	6	5	4	3	2	1	0	
LS_THRES_UP_0								0X21
LS_THRES_UP_1								0x22
0	0	0	0	LS_THRES_UP_2				0X23

LS_THRES_UP_x sets the upper threshold value for the LS interrupt. The Interrupt Controller compares the value in LS_THRES_UP_x against measured data in the DATA_x registers of the selected LS interrupt channel. It generates an interrupt event if DATA_x exceeds the threshold level.

The data format for LS_THRES_UP_x must match that of the DATA_x registers.

Reg 21HEX	Bit[7:0]	LS upper interrupt threshold value, LSB
Reg 22HEX	Bit[7:0]	LS upper interrupt threshold value, intervening byte
Reg 23HEX	Bit[3:0]	LS upper interrupt threshold value, MSB

LS_THRES_LOW

Default Value: 00HEX, 00HEX, 00HEX

7	6	5	4	3	2	1	0	
LS_THRES_LOW_0								0X24
LS_THRES_LOW_1								0x25
0	0	0	0	LS_THRES_LOW_2				0X26

LS_THRES_LOW_x sets the lower threshold value for the LS interrupt. The Interrupt Controller compares the value in LS_THRES_LOW_x against measured data in the DATA_x registers of the selected LS interrupt channel. It generates an interrupt event if the DATA_x is below the threshold level.

The data format for LS_THRES_LOW_x must match that of the DATA_x registers.

Reg 24HEX	Bit[7:0]	LS lower interrupt threshold value, LSB
Reg 25HEX	Bit[7:0]	LS lower interrupt threshold value, intervening byte
Reg 26HEX	Bit[3:0]	LS lower interrupt threshold value, MSB

LS_THRES_VAR

Default Value: 00HEX

7	6	5	4	3	2	1	0	
0	0	0	0	0	LS_THRES_ VAR			0X27

FIELD	BIT	DESCRIPTION
LS_THRES_VAR	2:0	000: new LS_DATA varies by 8 counts compared to previous result. 001: new LS_DATA varies by 16 counts compared to previous result. 010: new LS_DATA varies by 32 counts compared to previous result. 011: new LS_DATA varies by 64 counts compared to previous result. … 1111: new LS_DATA varies by 1024 counts compared to previous result.

Application Information Hardware

The application hardware circuit for using implementing UVS and ALS is simple with the APDS-9200 and is shown in following figure. The bypass capacitor is placed as close to the device package and is connected directly to the power source and to the ground, as shown in the following figure. It allows the AC component of the V_{DD} to pass through to ground. It is suggested to have bypass capacitor that have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents caused by internal logic switching.

Pull-up resistors, RSDA and RSCL, maintain the SDA and SCL lines at a high level when the bus is free and ensure the signals are pulled up from a low to a high level within the required rise time. A pull-up resistor, R_{INT}, is also required for the interrupt (INT), which functions as a wired-AND signal in a similar fashion to the SCL and SDA lines. A typical impedance value of 10 kΩ can be used.

For a complete description of I^2C maximum and minimum R1 and R2 values, please review the I^2C Specification at http://www.semiconductors.philips.com.

Figure 19 Application Hardware Circuit

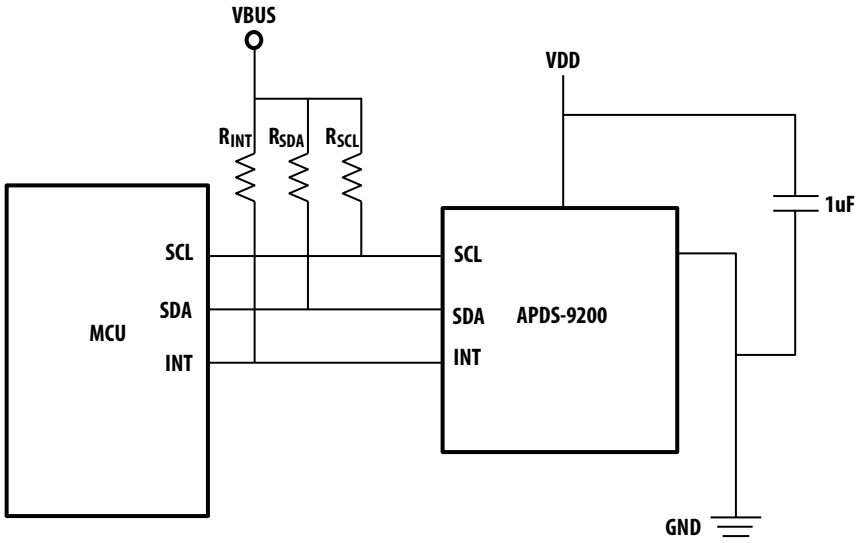
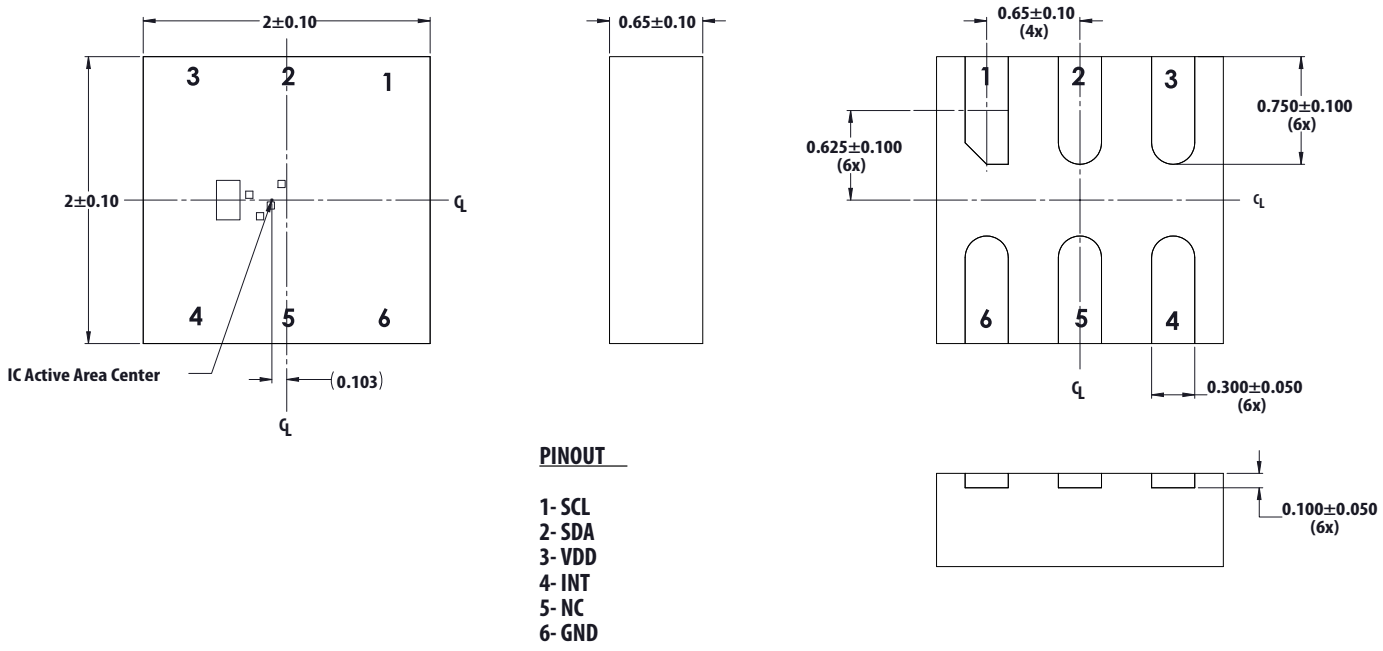
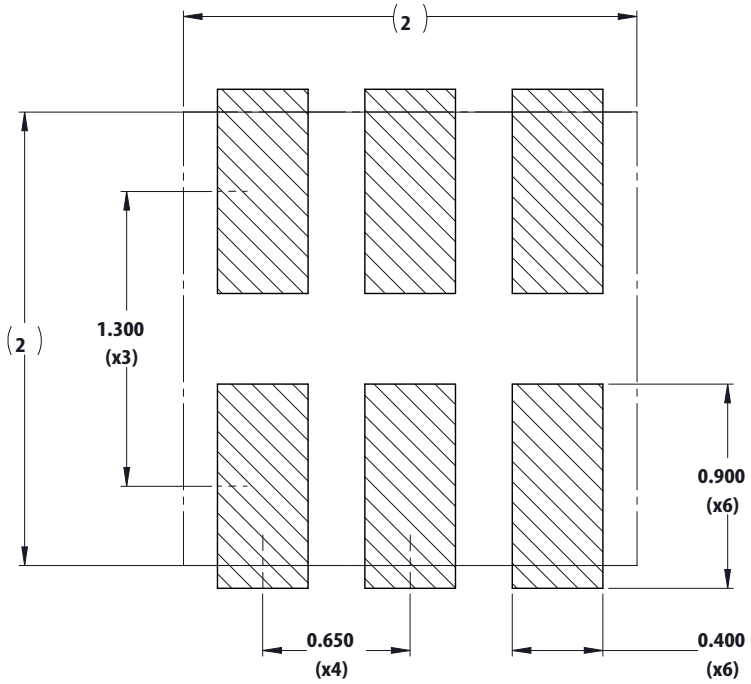


Figure 20 Package Outline Dimensions



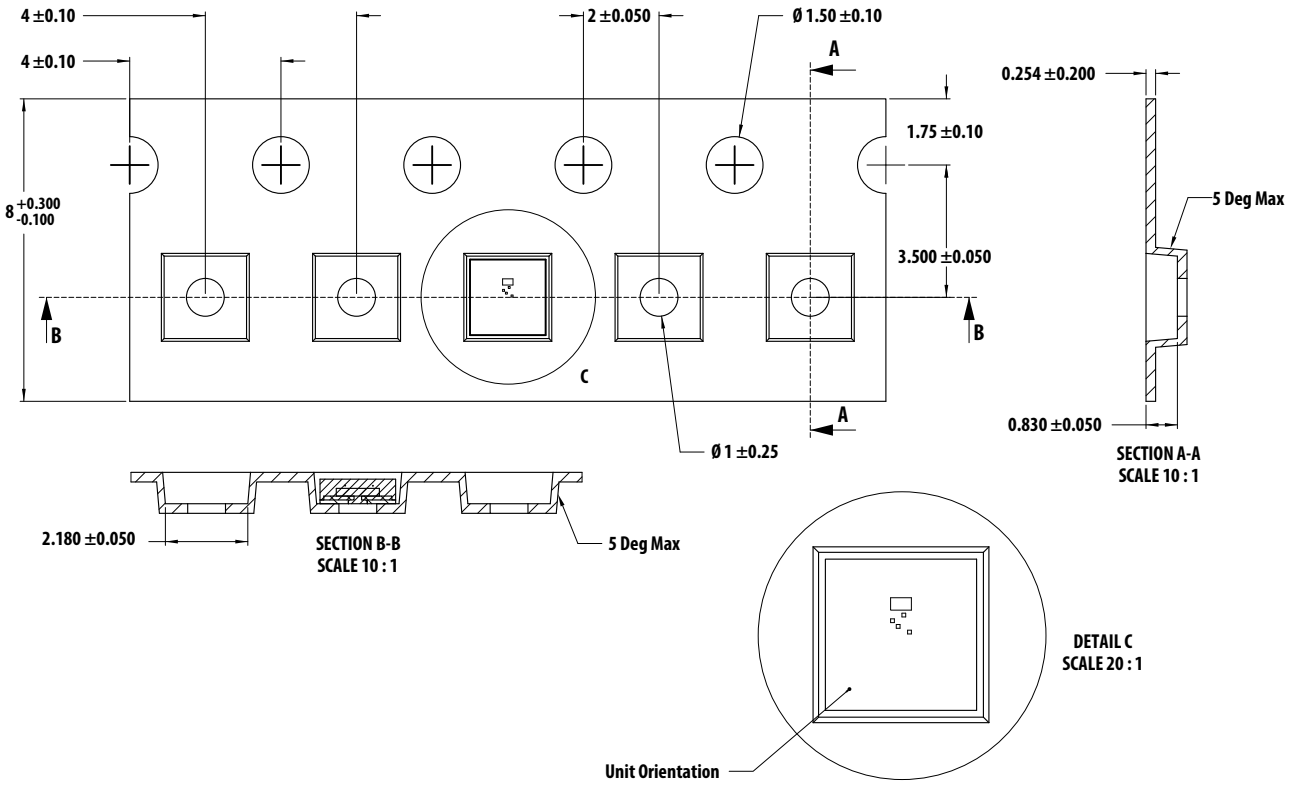
NOTE All dimensions are in millimeters.

Figure 21 PCB Pad Layout



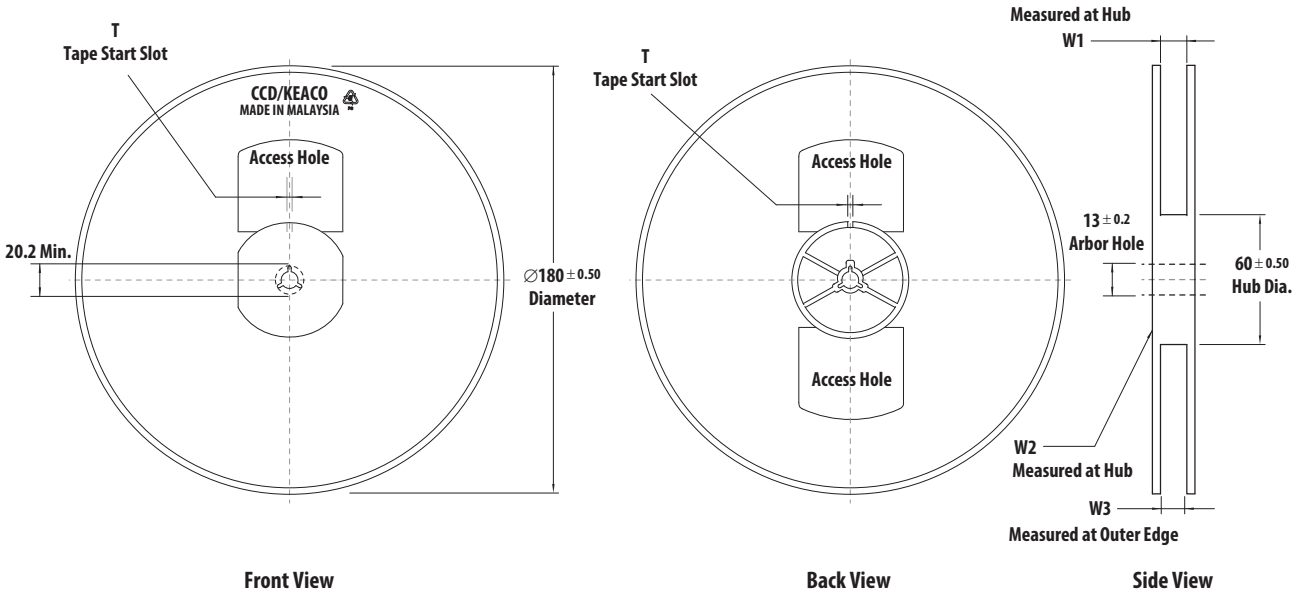
NOTE All dimensions are in millimeters.

Figure 22 Tape Dimensions



NOTE All dimensions are in millimeters.

Figure 23 Reel Dimensions



NOTE All dimensions are in millimeters.

Moisture Proof Packaging

All APDS-9200 options are shipped in moisture proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC MSL 3.

Figure 24 Moisture Proof Packaging

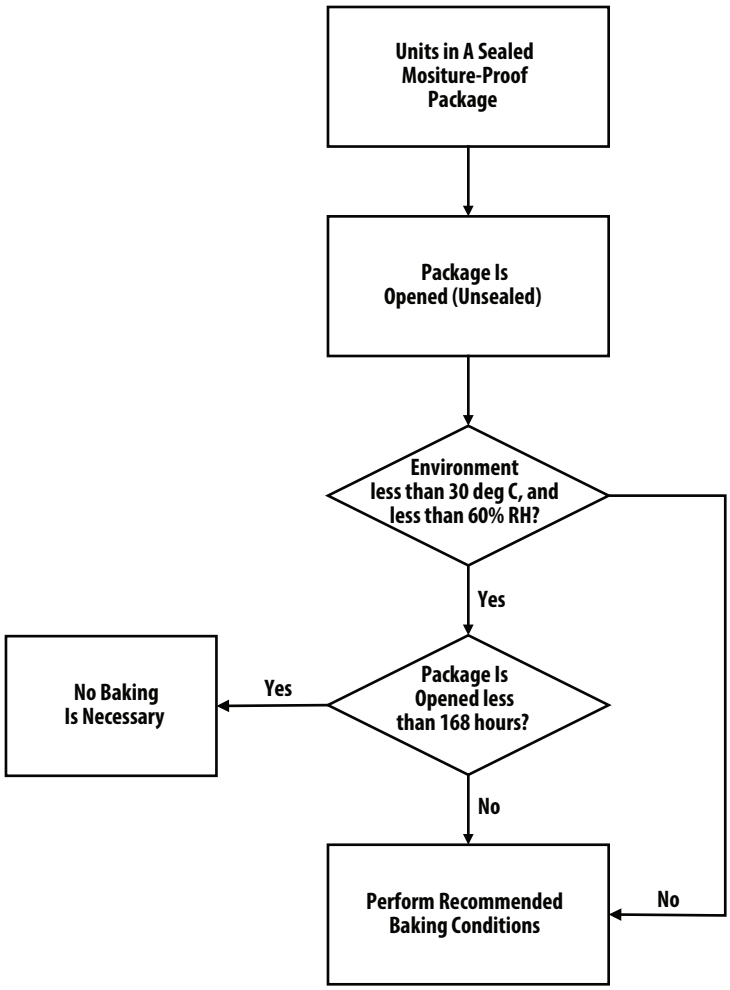


Table 8 Baking Conditions

Package	Temperature	Time
In Reel	60°C	48 hours
In Bulk	100°C	4 hours

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Baking should only be done once.

Table 9 Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from unsealing to soldering:

After removal from the bag, the parts should be soldered within 168 hours if stored at the recommended storage conditions. If times longer than 168 hours are needed, the parts must be stored in a dry box.

Figure 25 Recommended Reflow Profile

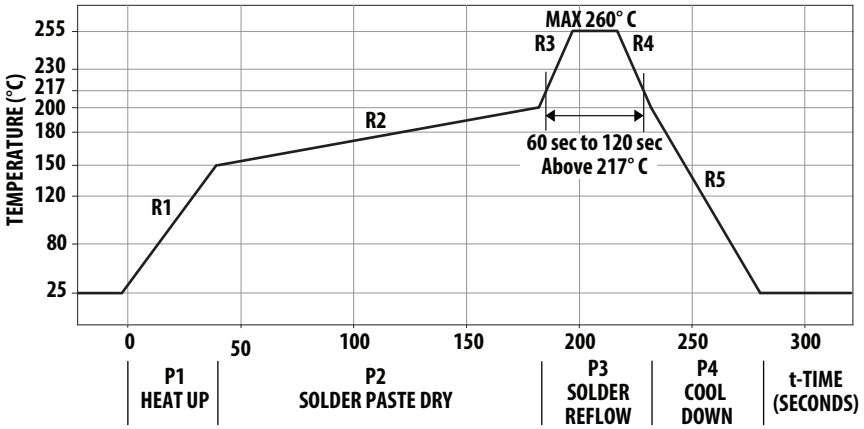


Table 10 Reflow Information

Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25°C to 150°C	3°C/s
Solder Paste Dry	P2, R2	150°C to 200°C	100 s to 180s
Solder Reflow	P3, R3 P3, R4	200°C to 260°C 260°C to 200°C	3°C/s –6°C/s
Cool Down	P4, R5	200°C to 25°C	–6 °C/s
Time maintained above liquidus point, 217°C		> 217°C	60s to 120s
Peak Temperature		260°C	—
Time within 5°C of actual Peak Temperature		> 255°C	20s to 40s
Time 25°C to Peak Temperature		25°C to 260°C	8 mins

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates or duration. The ΔT/Δtime rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In process zone P1, the PC board and component pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and component pins.

Process zone P2 should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260°C (500°F) for optimum results. The dwell time above the liquidus point of solder should be between 60 and 120 seconds. This is to assure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and component pins to change dimensions evenly, putting minimal stresses on the component.

It is recommended to perform reflow soldering no more than twice.

It is recommended to perform a calibration of the UVS ADC output against a calibrated UV test light source after final reflow and product assembly.

For product information and a complete list of distributors, please go to our web site: www.broadcom.com.

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RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product